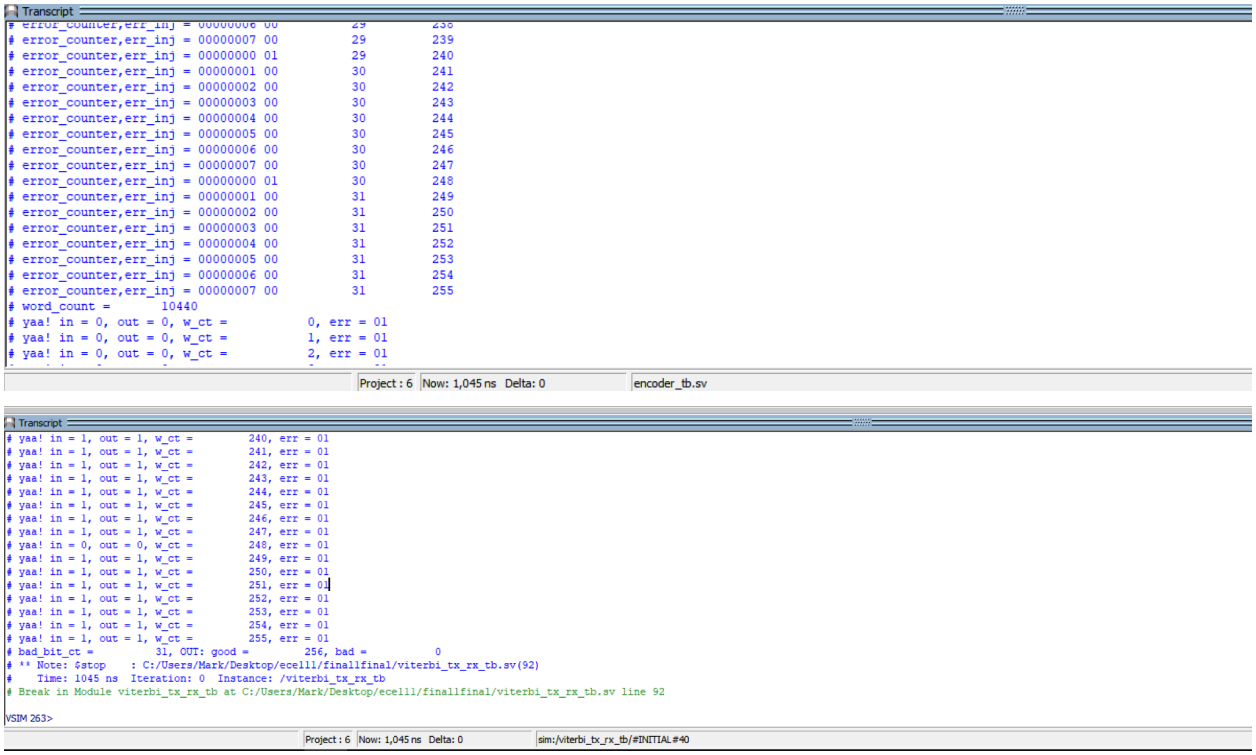
task	number of errors injected	patterns of errors injected	number of errors uncorrected
2a1	31	01	0
2a2	31	10	0
2a3	32	11	0
2a4	31	0101	0
2a5	31	1010	0
2a6	32	01010101	30
2a7	32	10101010	13
2a8	32	1111	21
2b1	31	01	0
2b2	37	10	3
2b3	30	11	14
2b4	33	0101	4
2b5	26	1010	6
2b6	20	01010101	3
2b7	20	10101010	0
2b8	14	1111	3
2c1	16	01	0
2c2	32	0101	0
2c3	48	010101	0
2c(output errors)	64	01010101	81
2d	64	10101010	30
2e	64	11111111	44

In both the 2a and 2b tests, I evaluated how the Viterbi decoder handled errors, but the way I injected errors was different. In 2a, I placed errors at fixed intervals using a specific bit error rate, so the error locations were predictable. In 2b, I introduced errors randomly with the same overall error rate, meaning the errors were scattered unpredictably. In tests 2a1 to 2a5, there were zero uncorrected errors because the errors injected were simple and spread out. We find that 2a1 only had two-bit errors, and in 2a2 and 2a3, also two bits were flipped. I think the errors were not close together. Since I assume this made it easy for the Viterbi decoder to fix them without any problems. The errors didn't cause the decoder to choose the wrong path because the path metrics stayed stable with such low-density errors. However, starting from 2a6, the errors became more frequent and complex, like in the "01010101" pattern. That lets the patterns have more bit errors. I found where errors happened almost every other bit. This higher density of errors made it harder for the decoder to keep track of the correct path, and it couldn't correct

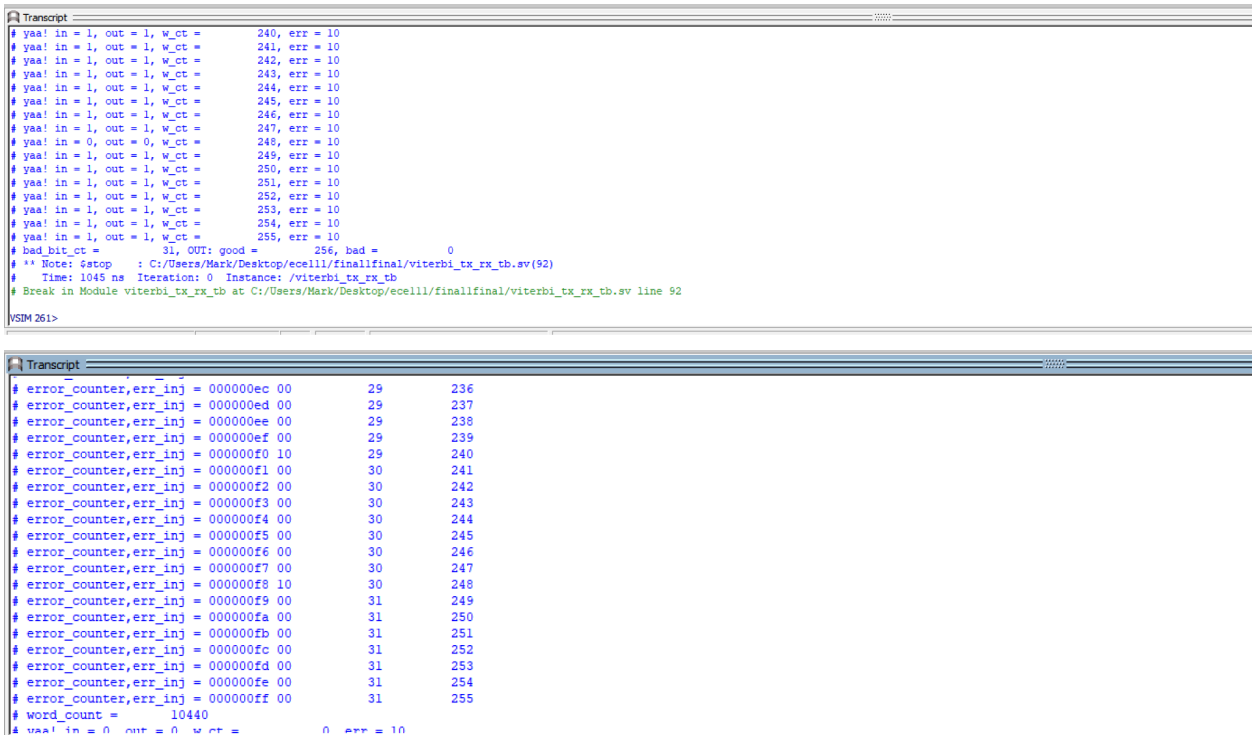
all of them, which is why uncorrected errors started to show up after 2a6. I was noticed that as the number of consecutive errors increased—from single-bit errors to bursts of up to four bits—the decoder had a harder time correcting them in both cases. However, the decoder generally performed better in the 2a tests because the fixed patterns made it easier to recover from errors. There was one exception, when I injected four consecutive error bits at a 1/32 rate, the random version in 2b actually corrected more errors than the fixed one in 2a. I think this happened because the random errors were spread out more by chance, which reduced the decoder's likelihood of choosing the wrong path. Hence, I could state that 2a part tests showed the decoder's performance in a controlled environment, then 2b reflected more unpredictable conditions.

In tests 2c to 2e, the goal was to find out how many errors the Viterbi decoder could handle before it started failing. In 2c1 to 2c3, the error patterns were still simple, like "01", "0101", and "010101", and even though more errors were injected, the decoder was still able to correct all of them with zero uncorrected errors. But when the error density increased further in 2c (output errors), with the "01010101" pattern and 64 errors injected, the decoder couldn't keep up anymore and there were 81 uncorrected errors. In 2d and 2e, the error patterns were even denser, like "10101010" and "11111111", and although the number of injected errors stayed the same at 64, the number of uncorrected errors was still very high, with 30 in 2d and 44 in 2e. These results show that when the number of errors goes beyond what the decoder can handle, especially when they are close together in time which is it quickly starts failing to correct them.

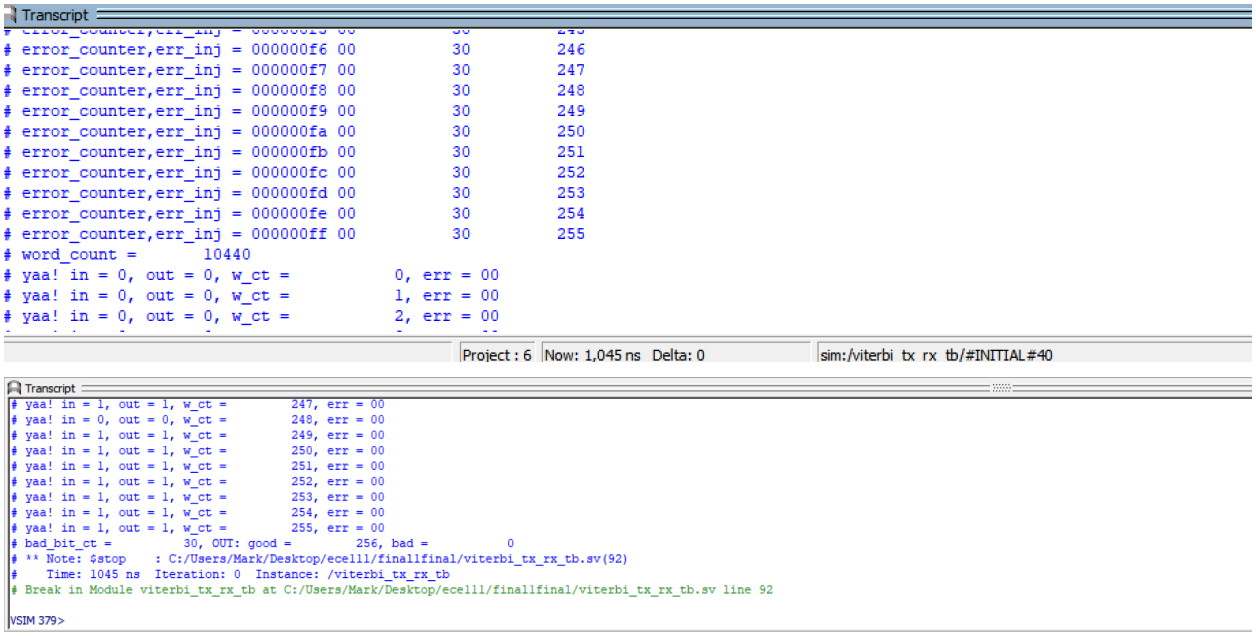
2a1


Transcript
error_counter,err_inj = 00000007 00 29 239
error_counter,err_inj = 00000000 01 29 240
error_counter,err_inj = 00000001 00 30 241
error_counter,err_inj = 00000002 00 30 242
error_counter,err_inj = 00000003 00 30 243
error_counter,err_inj = 00000004 00 30 244
error_counter,err_inj = 00000005 00 30 245
error_counter,err_inj = 00000006 00 30 246
error_counter,err_inj = 00000007 00 30 247
error_counter,err_inj = 00000000 01 30 248
error_counter,err_inj = 00000001 00 31 249
error_counter,err_inj = 00000002 00 31 250
error_counter,err_inj = 00000003 00 31 251
error_counter,err_inj = 00000004 00 31 252
error_counter,err_inj = 00000005 00 31 253
error_counter,err_inj = 00000006 00 31 254
error_counter,err_inj = 00000007 00 31 255
word_count = 10440
yaa! in = 0, out = 0, w_ct = 0, err = 01
yaa! in = 0, out = 0, w_ct = 1, err = 01
yaa! in = 0, out = 0, w_ct = 2, err = 01
Project : 6
Now: 1,045 ns Delta: 0
encoder_tb.sv
Transcript
yaa! in = 1, out = 1, w_ct = 240, err = 01
yaa! in = 1, out = 1, w_ct = 241, err = 01
yaa! in = 1, out = 1, w_ct = 242, err = 01
yaa! in = 1, out = 1, w_ct = 243, err = 01
yaa! in = 1, out = 1, w_ct = 244, err = 01
yaa! in = 1, out = 1, w_ct = 245, err = 01
yaa! in = 1, out = 1, w_ct = 246, err = 01
yaa! in = 1, out = 1, w_ct = 247, err = 01
yaa! in = 0, out = 0, w_ct = 248, err = 01
yaa! in = 1, out = 1, w_ct = 249, err = 01
yaa! in = 1, out = 1, w_ct = 250, err = 01
yaa! in = 1, out = 1, w_ct = 251, err = 01
yaa! in = 1, out = 1, w_ct = 252, err = 01
yaa! in = 1, out = 1, w_ct = 253, err = 01
yaa! in = 1, out = 1, w_ct = 254, err = 01
yaa! in = 1, out = 1, w_ct = 255, err = 01
bad_bit_ct = 31, OUT: good = 256, bad = 0
** Note: $stop : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92
VSIM 263>
Project : 6
Now: 1,045 ns Delta: 0
sim:/viterbi_tx_rx_tb/#INITIAL#40

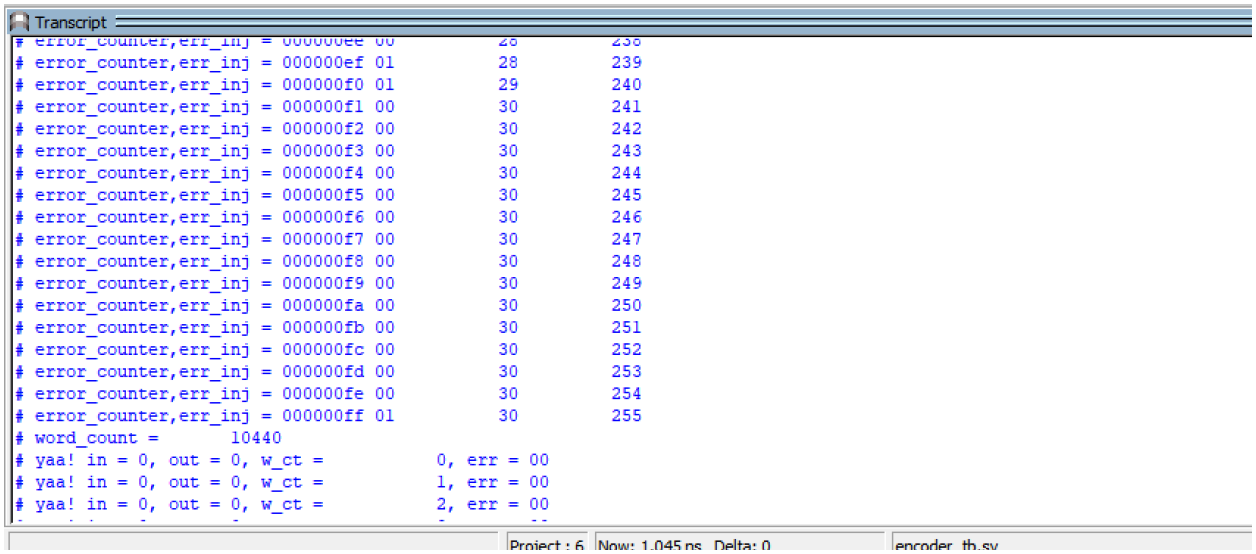
2a2

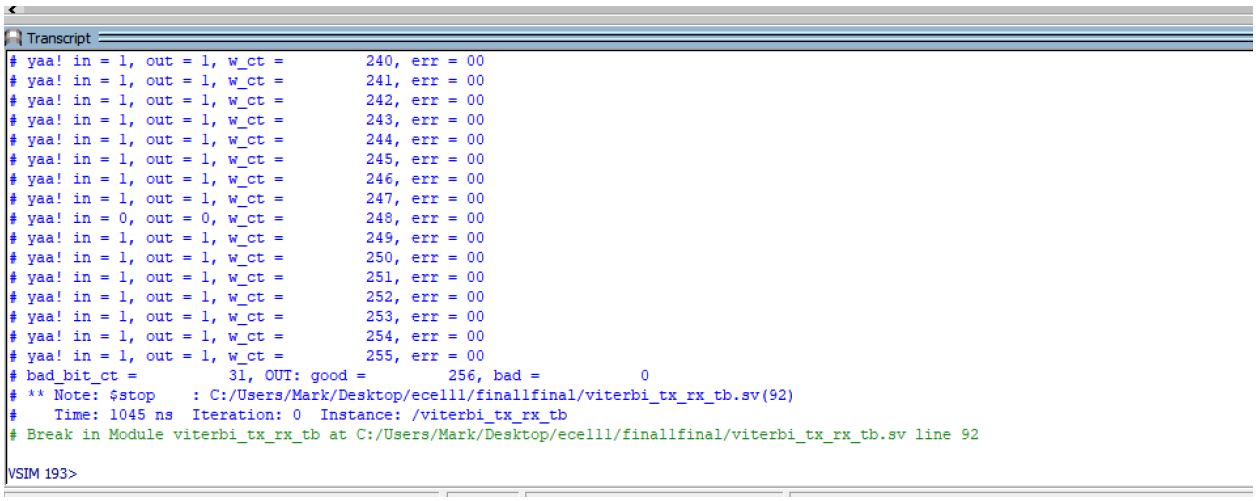

Transcript
yaa! in = 1, out = 1, w_ct = 240, err = 10
yaa! in = 1, out = 1, w_ct = 241, err = 10
yaa! in = 1, out = 1, w_ct = 242, err = 10
yaa! in = 1, out = 1, w_ct = 243, err = 10
yaa! in = 1, out = 1, w_ct = 244, err = 10
yaa! in = 1, out = 1, w_ct = 245, err = 10
yaa! in = 1, out = 1, w_ct = 246, err = 10
yaa! in = 1, out = 1, w_ct = 247, err = 10
yaa! in = 0, out = 0, w_ct = 248, err = 10
yaa! in = 1, out = 1, w_ct = 249, err = 10
yaa! in = 1, out = 1, w_ct = 250, err = 10
yaa! in = 1, out = 1, w_ct = 251, err = 10
yaa! in = 1, out = 1, w_ct = 252, err = 10
yaa! in = 1, out = 1, w_ct = 253, err = 10
yaa! in = 1, out = 1, w_ct = 254, err = 10
yaa! in = 1, out = 1, w_ct = 255, err = 10
bad_bit_ct = 31, OUT: good = 256, bad = 0
** Note: $stop : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92
VSIM 261>
Transcript
error_counter,err_inj = 000000ec 00 29 236
error_counter,err_inj = 000000ed 00 29 237
error_counter,err_inj = 000000ee 00 29 238
error_counter,err_inj = 000000ef 00 29 239
error_counter,err_inj = 000000f0 10 29 240
error_counter,err_inj = 000000f1 00 30 241
error_counter,err_inj = 000000f2 00 30 242
error_counter,err_inj = 000000f3 00 30 243
error_counter,err_inj = 000000f4 00 30 244
error_counter,err_inj = 000000f5 00 30 245
error_counter,err_inj = 000000f6 00 30 246
error_counter,err_inj = 000000f7 00 30 247
error_counter,err_inj = 000000f8 10 30 248
error_counter,err_inj = 000000f9 00 31 249
error_counter,err_inj = 000000fa 00 31 250
error_counter,err_inj = 000000fb 00 31 251
error_counter,err_inj = 000000fc 00 31 252
error_counter,err_inj = 000000fd 00 31 253
error_counter,err_inj = 000000fe 00 31 254
error_counter,err_inj = 000000ff 00 31 255
word_count = 10440

2a3

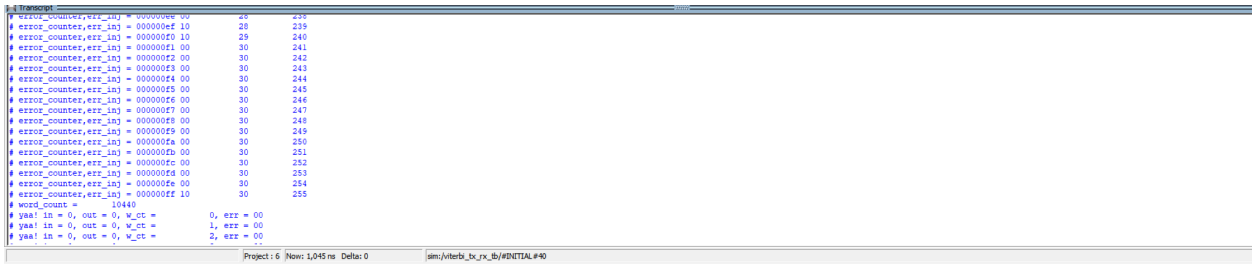

Transcript
error_counter,err_inj = 000000f6 00 30 246
error_counter,err_inj = 000000f7 00 30 247
error_counter,err_inj = 000000f8 00 30 248
error_counter,err_inj = 000000f9 00 30 249
error_counter,err_inj = 000000fa 00 30 250
error_counter,err_inj = 000000fb 00 30 251
error_counter,err_inj = 000000fc 00 30 252
error_counter,err_inj = 000000fd 00 30 253
error_counter,err_inj = 000000fe 00 30 254
error_counter,err_inj = 000000ff 00 30 255
word_count = 10440
yaa! in = 0, out = 0, w_ct = 0, err = 00
yaa! in = 0, out = 0, w_ct = 1, err = 00
yaa! in = 0, out = 0, w_ct = 2, err = 00
Project : 6
Now: 1,045 ns Delta: 0
sim:/viterbi_tx_rx_tb/#INITIAL#40
Transcript
yaa! in = 1, out = 1, w_ct = 247, err = 00
yaa! in = 0, out = 0, w_ct = 248, err = 00
yaa! in = 1, out = 1, w_ct = 249, err = 00
yaa! in = 1, out = 1, w_ct = 250, err = 00
yaa! in = 1, out = 1, w_ct = 251, err = 00
yaa! in = 1, out = 1, w_ct = 252, err = 00
yaa! in = 1, out = 1, w_ct = 253, err = 00
yaa! in = 1, out = 1, w_ct = 254, err = 00
yaa! in = 1, out = 1, w_ct = 255, err = 00
bad_bit_ct = 30, OUT: good = 256, bad = 0
** Note: $stop : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92
VSIM 379>

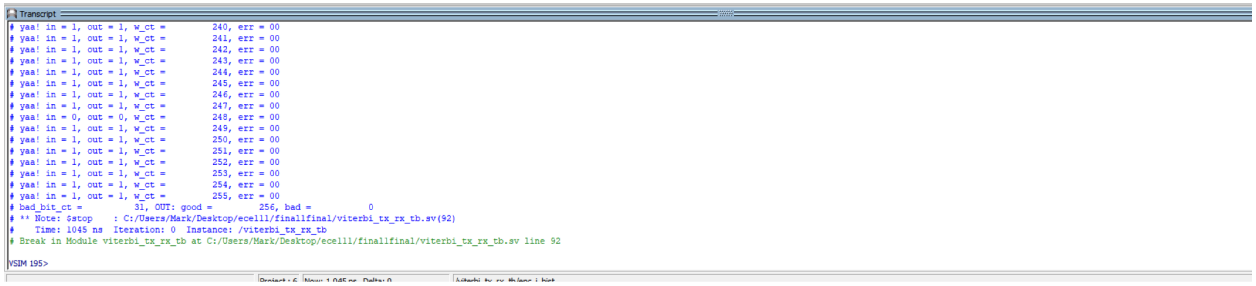
2a4


Transcript
error_counter,err_inj = 000000ee 00 28 238
error_counter,err_inj = 000000ef 01 28 239
error_counter,err_inj = 000000f0 01 29 240
error_counter,err_inj = 000000f1 00 30 241
error_counter,err_inj = 000000f2 00 30 242
error_counter,err_inj = 000000f3 00 30 243
error_counter,err_inj = 000000f4 00 30 244
error_counter,err_inj = 000000f5 00 30 245
error_counter,err_inj = 000000f6 00 30 246
error_counter,err_inj = 000000f7 00 30 247
error_counter,err_inj = 000000f8 00 30 248
error_counter,err_inj = 000000f9 00 30 249
error_counter,err_inj = 000000fa 00 30 250
error_counter,err_inj = 000000fb 00 30 251
error_counter,err_inj = 000000fc 00 30 252
error_counter,err_inj = 000000fd 00 30 253
error_counter,err_inj = 000000fe 00 30 254
error_counter,err_inj = 000000ff 01 30 255
word_count = 10440
yaa! in = 0, out = 0, w_ct = 0, err = 00
yaa! in = 0, out = 0, w_ct = 1, err = 00
yaa! in = 0, out = 0, w_ct = 2, err = 00
Project : 6
Now: 1,045 ns Delta: 0
encoder_tb.sv


Transcript
yaa! in = 1, out = 1, w_ct = 240, err = 00
yaa! in = 1, out = 1, w_ct = 241, err = 00
yaa! in = 1, out = 1, w_ct = 242, err = 00
yaa! in = 1, out = 1, w_ct = 243, err = 00
yaa! in = 1, out = 1, w_ct = 244, err = 00
yaa! in = 1, out = 1, w_ct = 245, err = 00
yaa! in = 1, out = 1, w_ct = 246, err = 00
yaa! in = 1, out = 1, w_ct = 247, err = 00
yaa! in = 0, out = 0, w_ct = 248, err = 00
yaa! in = 1, out = 1, w_ct = 249, err = 00
yaa! in = 1, out = 1, w_ct = 250, err = 00
yaa! in = 1, out = 1, w_ct = 251, err = 00
yaa! in = 1, out = 1, w_ct = 252, err = 00
yaa! in = 1, out = 1, w_ct = 253, err = 00
yaa! in = 1, out = 1, w_ct = 254, err = 00
yaa! in = 1, out = 1, w_ct = 255, err = 00
bad_bit_ct = 31, OUT: good = 256, bad = 0
** Note: $stop : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92
VSIM 193>

2a5


Transcript
Project : 6
Now: 1,045 ns Delta: 0
sim:/viterbi_tx_rx_tb/#INITIAL#40


Transcript
VSIM 195>

2a6

```
Transcript
# error_counter,err_inj = 000000d9 00          28          217
# error_counter,err_inj = 000000da 00          28          218
# error_counter,err_inj = 000000db 00          28          219
# error_counter,err_inj = 000000dc 00          28          220
# error_counter,err_inj = 000000dd 00          28          221
# error_counter,err_inj = 000000de 00          28          222
# error_counter,err_inj = 000000df 00          28          223
# error_counter,err_inj = 000000e0 00          28          224
# error_counter,err_inj = 000000e1 01          28          225
# error_counter,err_inj = 000000e2 01          29          226
# error_counter,err_inj = 000000e3 01          30          227
# error_counter,err_inj = 000000e4 01          31          228
# error_counter,err_inj = 000000e5 00          32          229
# error_counter,err_inj = 000000e6 00          32          230
# error_counter,err_inj = 000000e7 00          32          231
# error_counter,err_inj = 000000e8 00          32          232
# error_counter,err_inj = 000000e9 00          32          233
# error_counter,err_inj = 000000ea 00          32          234
# error_counter,err_inj = 000000eb 00          32          235
# error_counter,err_inj = 000000ec 00          32          236
# error_counter,err_inj = 000000ed 00          32          237
# error_counter,err_inj = 000000ee 00          32          238
```

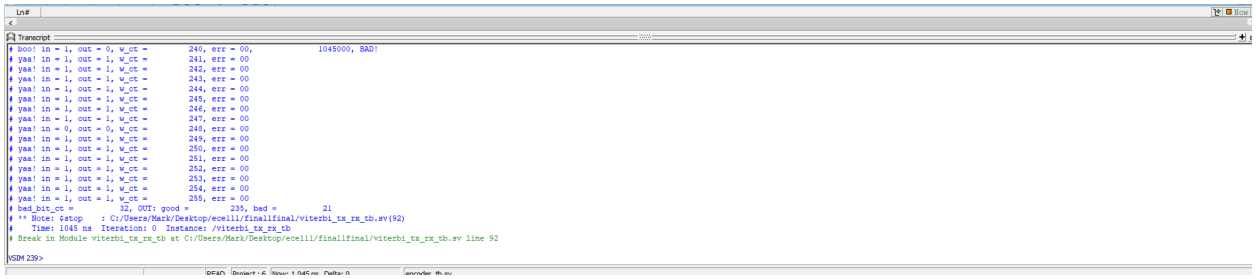
```
Transcript
# yaa! in = 1, out = 1, w_ct =         240, err = 00
# yaa! in = 1, out = 1, w_ct =         241, err = 00
# yaa! in = 1, out = 1, w_ct =         242, err = 00
# yaa! in = 1, out = 1, w_ct =         243, err = 00
# yaa! in = 1, out = 1, w_ct =         244, err = 00
# yaa! in = 1, out = 1, w_ct =         245, err = 00
# yaa! in = 1, out = 1, w_ct =         246, err = 00
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          32, OUT: good =         226, bad =          30
# ** Note: $stop    : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 219>
```

2a7

```
Transcript
# error_counter,err_inj = 000000d9 00          28          217
# error_counter,err_inj = 000000da 00          28          218
# error_counter,err_inj = 000000db 00          28          219
# error_counter,err_inj = 000000dc 00          28          220
# error_counter,err_inj = 000000dd 00          28          221
# error_counter,err_inj = 000000de 00          28          222
# error_counter,err_inj = 000000df 00          28          223
# error_counter,err_inj = 000000e0 00          28          224
# error_counter,err_inj = 000000e1 10          28          225
# error_counter,err_inj = 000000e2 10          29          226
# error_counter,err_inj = 000000e3 10          30          227
# error_counter,err_inj = 000000e4 10          31          228
# error_counter,err_inj = 000000e5 00          32          229
# error_counter,err_inj = 000000e6 00          32          230
# error_counter,err_inj = 000000e7 00          32          231
# error_counter,err_inj = 000000e8 00          32          232
# error_counter,err_inj = 000000e9 00          32          233
# error_counter,err_inj = 000000ea 00          32          234
# error_counter,err_inj = 000000eb 00          32          235
# error_counter,err_inj = 000000ec 00          32          236
# error_counter,err_inj = 000000ed 00          32          237
# error_counter,err_inj = 000000ee 00          32          238
```

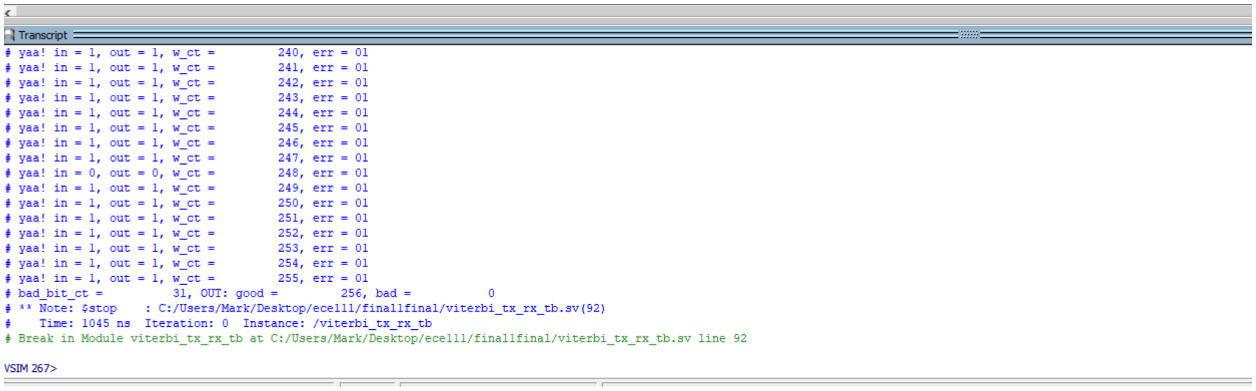
```
Transcript
# boo! in = 1, out = 0, w_ct =         240, err = 00,              1045000, BAD!
# yaa! in = 1, out = 1, w_ct =         241, err = 00
# yaa! in = 1, out = 1, w_ct =         242, err = 00
# yaa! in = 1, out = 1, w_ct =         243, err = 00
# yaa! in = 1, out = 1, w_ct =         244, err = 00
# yaa! in = 1, out = 1, w_ct =         245, err = 00
# yaa! in = 1, out = 1, w_ct =         246, err = 00
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          32, OUT: good =         243, bad =          13
# ** Note: $stop    : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92
```

2a8

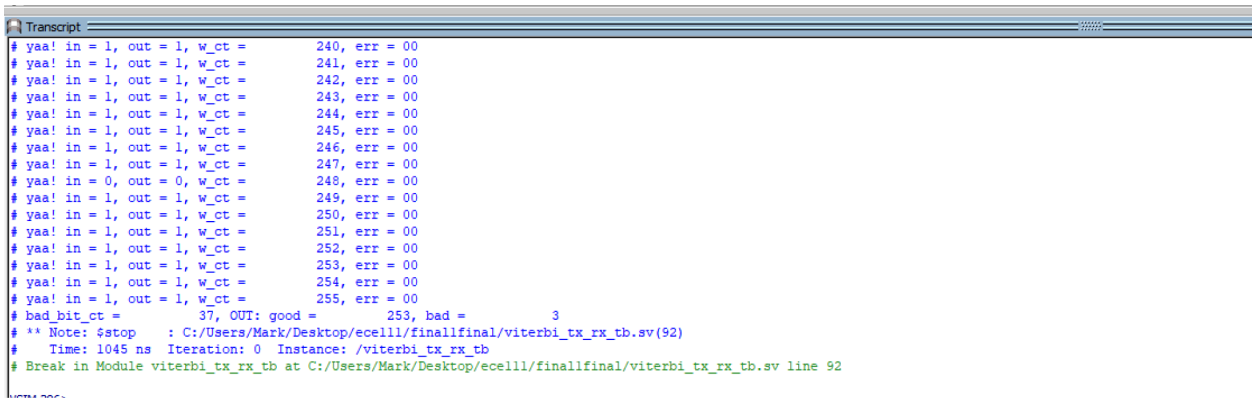

Transcript
boo! in = 1, out = 0, w_ct = 240, err = 00, 1045000, BAD!
yaa! in = 1, out = 1, w_ct = 241, err = 00
yaa! in = 1, out = 1, w_ct = 242, err = 00
yaa! in = 1, out = 1, w_ct = 243, err = 00
yaa! in = 1, out = 1, w_ct = 244, err = 00
yaa! in = 1, out = 1, w_ct = 245, err = 00
yaa! in = 1, out = 1, w_ct = 246, err = 00
yaa! in = 1, out = 1, w_ct = 247, err = 00
yaa! in = 0, out = 0, w_ct = 248, err = 00
yaa! in = 1, out = 1, w_ct = 249, err = 00
yaa! in = 1, out = 1, w_ct = 250, err = 00
yaa! in = 1, out = 1, w_ct = 251, err = 00
yaa! in = 1, out = 1, w_ct = 252, err = 00
yaa! in = 1, out = 1, w_ct = 253, err = 00
yaa! in = 1, out = 1, w_ct = 254, err = 00
yaa! in = 1, out = 1, w_ct = 255, err = 00
bad_bit_ct = 32, OUT: good = 235, bad = 21
** Note: $stop : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92
VSIM 239>


Transcript
error_counter,err_inj = 000000dc 00 28 220
error_counter,err_inj = 000000dd 00 28 221
error_counter,err_inj = 000000de 00 28 222
error_counter,err_inj = 000000df 00 28 223
error_counter,err_inj = 000000e0 00 28 224
error_counter,err_inj = 000000e1 00 28 225
error_counter,err_inj = 000000e2 00 28 226
error_counter,err_inj = 000000e3 11 28 227
error_counter,err_inj = 000000e4 11 30 228
error_counter,err_inj = 000000e5 00 32 229
error_counter,err_inj = 000000e6 00 32 230
error_counter,err_inj = 000000e7 00 32 231
error_counter,err_inj = 000000e8 00 32 232
error_counter,err_inj = 000000e9 00 32 233
error_counter,err_inj = 000000ea 00 32 234
error_counter,err_inj = 000000eb 00 32 235
error_counter,err_inj = 000000ec 00 32 236
error_counter,err_inj = 000000ed 00 32 237
error_counter,err_inj = 000000ee 00 32 238
error_counter,err_inj = 000000ef 00 32 239

2b1


Transcript
yaa! in = 1, out = 1, w_ct = 240, err = 01
yaa! in = 1, out = 1, w_ct = 241, err = 01
yaa! in = 1, out = 1, w_ct = 242, err = 01
yaa! in = 1, out = 1, w_ct = 243, err = 01
yaa! in = 1, out = 1, w_ct = 244, err = 01
yaa! in = 1, out = 1, w_ct = 245, err = 01
yaa! in = 1, out = 1, w_ct = 246, err = 01
yaa! in = 1, out = 1, w_ct = 247, err = 01
yaa! in = 0, out = 0, w_ct = 248, err = 01
yaa! in = 1, out = 1, w_ct = 249, err = 01
yaa! in = 1, out = 1, w_ct = 250, err = 01
yaa! in = 1, out = 1, w_ct = 251, err = 01
yaa! in = 1, out = 1, w_ct = 252, err = 01
yaa! in = 1, out = 1, w_ct = 253, err = 01
yaa! in = 1, out = 1, w_ct = 254, err = 01
yaa! in = 1, out = 1, w_ct = 255, err = 01
bad_bit_ct = 31, OUT: good = 256, bad = 0
** Note: $stop : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92
VSIM 267>

2b2


Transcript
yaa! in = 1, out = 1, w_ct = 240, err = 00
yaa! in = 1, out = 1, w_ct = 241, err = 00
yaa! in = 1, out = 1, w_ct = 242, err = 00
yaa! in = 1, out = 1, w_ct = 243, err = 00
yaa! in = 1, out = 1, w_ct = 244, err = 00
yaa! in = 1, out = 1, w_ct = 245, err = 00
yaa! in = 1, out = 1, w_ct = 246, err = 00
yaa! in = 1, out = 1, w_ct = 247, err = 00
yaa! in = 0, out = 0, w_ct = 248, err = 00
yaa! in = 1, out = 1, w_ct = 249, err = 00
yaa! in = 1, out = 1, w_ct = 250, err = 00
yaa! in = 1, out = 1, w_ct = 251, err = 00
yaa! in = 1, out = 1, w_ct = 252, err = 00
yaa! in = 1, out = 1, w_ct = 253, err = 00
yaa! in = 1, out = 1, w_ct = 254, err = 00
yaa! in = 1, out = 1, w_ct = 255, err = 00
bad_bit_ct = 37, OUT: good = 253, bad = 3
** Note: $stop : C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv(92)
Time: 1045 ns Iteration: 0 Instance: /viterbi_tx_rx_tb
Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ece111/finallfinal/viterbi_tx_rx_tb.sv line 92

2b3

```
Transcript
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          30, OUT: good =         242, bad =          14
# ** Note: $stop    : C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 381>
```

2b4

```
Transcript
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          33, OUT: good =         252, bad =           4
# ** Note: $stop    : C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 383>
```

2b5

```
Transcript
# yaa! in = 1, out = 1, w_ct =         240, err = 00
# yaa! in = 1, out = 1, w_ct =         241, err = 00
# yaa! in = 1, out = 1, w_ct =         242, err = 00
# yaa! in = 1, out = 1, w_ct =         243, err = 00
# yaa! in = 1, out = 1, w_ct =         244, err = 00
# yaa! in = 1, out = 1, w_ct =         245, err = 00
# yaa! in = 1, out = 1, w_ct =         246, err = 00
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          26, OUT: good =         250, bad =           6
# ** Note: $stop    : C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 355>
```

2b6

```
Transcript
# yaa! in = 1, out = 1, w_ct =         240, err = 00
# yaa! in = 1, out = 1, w_ct =         241, err = 00
# yaa! in = 1, out = 1, w_ct =         242, err = 00
# yaa! in = 1, out = 1, w_ct =         243, err = 00
# yaa! in = 1, out = 1, w_ct =         244, err = 00
# yaa! in = 1, out = 1, w_ct =         245, err = 00
# yaa! in = 1, out = 1, w_ct =         246, err = 00
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          20, OUT: good =         253, bad =           3
# ** Note: $stop    : C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecel11/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 377>
```

2b7

```
# yaa! in = 1, out = 1, w_ct =         240, err = 00
# yaa! in = 1, out = 1, w_ct =         241, err = 00
# yaa! in = 1, out = 1, w_ct =         242, err = 00
# yaa! in = 1, out = 1, w_ct =         243, err = 00
# yaa! in = 1, out = 1, w_ct =         244, err = 00
# yaa! in = 1, out = 1, w_ct =         245, err = 00
# yaa! in = 1, out = 1, w_ct =         246, err = 00
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          20, OUT: good =         256, bad =           0
# ** Note: $stop    : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92
```

2b8

```
Transcript
# yaa! in = 1, out = 1, w_ct =         240, err = 00
# yaa! in = 1, out = 1, w_ct =         241, err = 00
# yaa! in = 1, out = 1, w_ct =         242, err = 00
# yaa! in = 1, out = 1, w_ct =         243, err = 00
# yaa! in = 1, out = 1, w_ct =         244, err = 00
# yaa! in = 1, out = 1, w_ct =         245, err = 00
# yaa! in = 1, out = 1, w_ct =         246, err = 00
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# yaa! in = 1, out = 1, w_ct =         250, err = 00
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          14, OUT: good =         253, bad =           3
# ** Note: $stop    : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92

/SIM 359>
```

2c

```
Transcript
# boo! in = 1, out = 0, w_ct =         247, err = 00,              1045000, BAD!
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# boo! in = 1, out = 0, w_ct =         250, err = 00,              1045000, BAD!
# boo! in = 1, out = 0, w_ct =         251, err = 00,              1045000, BAD!
# boo! in = 1, out = 0, w_ct =         252, err = 00,              1045000, BAD!
# boo! in = 1, out = 0, w_ct =         253, err = 00,              1045000, BAD!
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          64, OUT: good =         175, bad =          81
# ** Note: $stop    : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 393>
```

2d

```
Transcript
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# boo! in = 1, out = 0, w_ct =         250, err = 00,              1045000, BAD!
# yaa! in = 1, out = 1, w_ct =         251, err = 00
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# yaa! in = 1, out = 1, w_ct =         255, err = 00
# bad_bit_ct =          64, OUT: good =         226, bad =          30
# ** Note: $stop    : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92

/SIM 395>
```

Ln: 92 Col: 0 | READ | Project : 6 | Now: 1,045 ns Delta: 0 | sim:/viterbi_tx_rx_tb/#INITIAL#40

2e

```
Transcript
# yaa! in = 1, out = 1, w_ct =         247, err = 00
# yaa! in = 0, out = 0, w_ct =         248, err = 00
# yaa! in = 1, out = 1, w_ct =         249, err = 00
# boo! in = 1, out = 0, w_ct =         250, err = 00,              1045000, BAD!
# boo! in = 1, out = 0, w_ct =         251, err = 00,              1045000, BAD!
# yaa! in = 1, out = 1, w_ct =         252, err = 00
# yaa! in = 1, out = 1, w_ct =         253, err = 00
# yaa! in = 1, out = 1, w_ct =         254, err = 00
# boo! in = 1, out = 0, w_ct =         255, err = 00,              1045000, BAD!
# bad_bit_ct =          64, OUT: good =         212, bad =          44
# ** Note: $stop    : C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv(92)
#    Time: 1045 ns  Iteration: 0  Instance: /viterbi_tx_rx_tb
# Break in Module viterbi_tx_rx_tb at C:/Users/Mark/Desktop/ecelll/finallfinal/viterbi_tx_rx_tb.sv line 92

VSIM 416>
```